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10/533,056	10/03/2005	Jun-ichi Okamura	1032-0001WOUS	9035

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EXAMINER	
LAM, KENNETH T	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/533,056	OKAMURA, JUN-ICHI	
	Examiner	Art Unit	
	KENNETH LAM	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 October 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/27/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 5-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites the limitation "the low pass filter" in page 32 line 34. There is insufficient antecedent basis for this limitation in the claim.

Claim 6 recites the limitation "the low pass filter" in page 33 line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the low pass filter" in page 33 line 8. There is insufficient antecedent basis for this limitation in the claim.

Claim 8 recites the limitation "the low pass filter" in page 33 line 15. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 4, 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Okamura (WO 02/065690).

Re Claim 1, Okamura discloses a receiver apparatus having a demodulator circuit that demodulates transmitted serial data into parallel data by sampling the transmitted serial data on the basis of first and second clock signals having different numbers of clocks to be output in synchronization with a cycle of a transmitted clock, said receiver apparatus comprising:

a first synchronizing circuit (First DLL circuit 110, Figure 10) generating the first clock signal synchronized with the cycle of the transmitted clock; and

a second synchronizing circuit (Second DLL circuit 120, Figure 10) generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal,

wherein the demodulator circuit comprises the second synchronizing circuit, a sampling register (Sampling Circuit 130, Figure 10) storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit (Phase Alignment Circuit 60, Figure 10) that calculates a difference between the transmitted serial data and the input clock signal on the basis of the sampled data, and a clock select circuit (Clock signal selection circuit 70, Figure 10) that adjusts a phase of a symbol-sampled signal on the basis of the difference.

Re Claim 4, Okamura discloses the receiver apparatus as claimed in claim 1, wherein the first synchronizing circuit inputs the first clock signal into at least two said synchronizing circuits (Figure 10).

Re Claim 11, Okamura discloses the receiver apparatus as claimed in claim 1, wherein the clock select circuit (Clock signal selection circuit 70, Figure 10) selects multiple clocks synchronized with the transmitted clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference calculating circuit in order to adjust a phase relation of the transmitted clock in synchronization with the cycle of the transmitted clock.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in **Graham v. John Deere Co., 383 U.S. 1, 148 USPQ 459 (1966)**, that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows: ***(See MPEP Ch. 2141)***

a. Determining the scope and contents of the prior art;
b. Ascertaining the differences between the prior art and the claims in issue;
c. Resolving the level of ordinary skill in the pertinent art; and
d. Evaluating evidence of secondary considerations for indicating obviousness or nonobviousness.

6. Claims 2-3, 5-8, 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamura (WO 02/065690) in view of Nakamura (US 2002/0154723 A1).

Re Claim 2, Okamura discloses a receiver apparatus having at least two demodulator circuits that demodulate transmitted serial data into parallel data by sampling the transmitted serial data on the basis of first and second clock signals having different numbers of clocks to be output in synchronization with a cycle of a transmitted clock, said receiver apparatus comprising:

a first synchronizing circuit (First DLL circuit 110, Figure 10) generating the first clock signal synchronized with the cycle of the transmitted clock; and

a plurality of second synchronizing circuits (Second DLL circuit 120, Figure 10) generating the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal;

wherein:

each of said at least two demodulator circuits (Circuit Block 100 R G B, Figure 10) comprises any one of said plurality of second synchronizing circuits, a sampling register (Sampling Circuit 130, Figure 10) storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit (Phase Alignment Circuit 60, Figure 10) that calculates a difference between the transmitted serial data and the input clock signal on the basis of

a sampled data, and a clock select circuit (Clock signal selection circuit 70, Figure 10) that adjusts a phase of a symbol-sampled signal on the basis of the difference.

Okamura discloses the claimed invention except explicitly teaches a lowpass filter circuit in plurality of demodulator circuits. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops wherein,

a lowpass filter circuit (Low Pass Filter 50 56, Figure 5) included in one of said at least two modulator circuits is shared by another modulator circuit as the lowpass filter ([0130], [0131]).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a low pass filter circuit in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 3, Okamura discloses the receiver apparatus as claimed in claim 1 except explicitly teaches a phase detection circuit. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops wherein at least two said second synchronizing circuits share a phase detection circuit (Phase-Frequency Comparator 46, Figure 5).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a phase detection circuit in DLL or

PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 5, Okamura discloses the receiver apparatus as claimed in claim 1 except explicitly teaches a voltage control oscillator. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops comprising a voltage control oscillator (VCO 42, Figure 5) that generates the second clock signal on the basis of a controlled voltage output.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a VCO in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 6, Okamura discloses the receiver apparatus as claimed in claim 1 except explicitly discloses a voltage control delay circuit. However, Nakamura teaches an oversampling clock recovery method comprising a voltage control delay circuit (VCD 52, Figure 5) that generates the second clock signal on the basis of a controlled voltage output.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a VCD in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal

quality.

Re Claim 7, Okamura discloses the receiver apparatus as claimed in claim 1, further comprising a phase locked loop circuit or a delay locked loop circuit that includes the lowpass filter to be shared (DLL circuit, Figure 10).

Okamura discloses the claimed invention except explicitly teaches a lowpass filter circuit in plurality of demodulator circuits. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops comprising a lowpass filter (Low Pass Filter 50 56, Figure 5).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a low pass filter circuit in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 8, Okamura discloses the receiver apparatus as claimed in claim 1, wherein the first synchronizing circuit includes a phase locked loop circuit, and the second synchronizing circuit includes a delay locked loop circuit having the lowpass filter to be shared (DLL circuit, Figure 10).

Okamura discloses the claimed invention except explicitly teaches a lowpass filter circuit in plurality of demodulator circuits. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops comprising a lowpass filter (Low Pass Filter 50 56, Figure 5).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a low pass filter circuit in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 13, Okamura discloses a receiver apparatus comprising:

a first synchronizing circuit (First DLL circuit 110, Figure 10) generating a first clock signal synchronized with a cycle of a transmitted clock; and

a plurality of demodulator circuits (Circuit Block 100 R G B, Figure 10),

wherein:

each of said plurality of demodulator circuits includes a second synchronizing circuit generating (Second DLL circuit 120, Figure 10) the second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal, a sampling register (Sampling Circuit 130, Figure 10) storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit (Phase Alignment Circuit 60, Figure 10) that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit (Clock signal selection circuit 70, Figure 10) that selects multiple clocks synchronized with the transmission clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference

calculating circuit in order to adjust a phase relation of the transmission clock while synchronized with the cycle of the transmitted clock.

Okamura discloses the claimed invention except explicitly teaches a lowpass filter circuit in plurality of demodulator circuits. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops wherein,

at least one of the second synchronizing circuit included in each of said plurality of demodulator circuits generates the second clock signal on the basis of a controlled voltage output from a lowpass filter circuit (Low Pass Filter 50 56, Figure 5) included in the second synchronizing circuit in another demodulator circuit ([0130], [0131]).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a low pass filter circuit in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 14, Okamura discloses a receiver apparatus comprising:

a first synchronizing circuit (First DLL circuit 110, Figure 10) generating a first clock signal synchronized with a cycle of a transmitted clock; and

a plurality of demodulator circuits (Circuit Block 100 R G B, Figure 10),

wherein:

each of said plurality of demodulator circuits includes a second synchronizing circuit (Second DLL circuit 120, Figure 10) generating the second clock signal

synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal, a sampling register (Sampling Circuit 130, Figure 10) storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit (Phase Alignment Circuit 60, Figure 10) that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit (Clock signal selection circuit 70, Figure 10) that selects multiple clocks synchronized with the transmission clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the difference calculating circuit in order to adjust a phase relation of the transmission clock while the second synchronizing circuit is being synchronized with the cycle of the transmitted clock.

Okamura discloses the claimed invention except explicitly teaches a lowpass filter circuit in plurality of demodulator circuits. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops wherein,

at least one of the second synchronizing circuit included in each of said plurality of demodulator circuits includes a lowpass filter circuit (Low Pass Filter 50 56, Figure 5), supplies an output from the lowpass filter circuit to another demodulator circuit, and generates the second clock signal on the basis of a controlled voltage output from the lowpass filter circuit included in the second synchronizing circuit in another demodulator circuit ([0130]-[0131]).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to recognize the utilization of a low pass filter circuit in DLL or PLL as disclosed by Nakamura in order to achieve the same expected results and further improve the signal quality.

Re Claim 15, Okamura discloses a receiver apparatus comprising:

a first synchronizing circuit (First DLL circuit 110, Figure 10) generating a first clock signal synchronized with a cycle of a transmitted clock;

a demodulator circuit (Circuit Block 100R, Figure 10) that includes a second synchronizing circuit (Second DLL circuit 120, Figure 10) that generates a second clock signal on the basis of the controlled voltage output from the controlled voltage output circuit, a sampling register (Sampling Circuit 130, Figure 10) storing sampled data obtained by sampling the transmitted serial data on the basis of the first and second clock signals, a difference calculating circuit (Phase Alignment Circuit 60, Figure 10) that calculates a difference between the transmitted serial data and the transmitted clock on the basis of the sampled data, and a clock select circuit (Clock signal selection circuit 70, Figure 10) selects multiple clocks synchronized with the transmitted clock and deviated in phase to be the input clock signal of the second synchronizing circuit.

Okamura discloses the claimed invention except explicitly teaches a controlled voltage output circuit and clock select circuit selects clock phase based on the controlled voltage output circuit. However, Nakamura teaches an oversampling clock recovery method comprising phase locked loop and delay locked loops wherein,

a controlled voltage output circuit (Voltage-controlled delay line 52, Figure 5) that outputs a controlled voltage to generate a second clock signal synchronized with the cycle of the transmitted clock and having a number of clocks different from that of the first clock signal ([0134]); and

clock select circuit (Selector, Figure 12) selects multiple clocks synchronized with the transmitted clock and deviated in phase to be the input clock signal of the second synchronizing circuit, on the basis of an output from the controlled voltage output circuit in order to adjust a phase relation of the transmitted clock while synchronized with the cycle of the transmitted clock ([0143], [0252]-[0258]).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize the delay locked loops as taught by Nakamura with the receiver apparatus as taught by Okamura to achieve the same expected results and to further improve the accuracy in high-speed data transmission.

7. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamura (WO 02/065690).

Re Claim 9, Okamura discloses the receiver apparatus as claimed in claim 1, except explicitly teaches wherein the second synchronizing circuit generates the second clock signal having an n number of phases that satisfies n/m-1<1/3, where the first clock signal has the n number of phases and the second clock signal has an m number of phases. It would have been obvious to one having ordinary skill in the art at the time

the invention was made to formulate the number of phases, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 f.2d 272, 205 USPQ (CCPA 1980).

Re Claim 10, Okamura discloses the receiver apparatus as claimed in claim 1, except explicitly teaches wherein the second synchronizing circuit generates the second clock signal having an m number of phases that satisfies n/m-1<1/3, where the first clock signal has an n number of phases and the second clock signal has the m number of phases. It would have been obvious to one having ordinary skill in the art at the time the invention was made to formulate the number of phases, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. In re Boesch, 617 f.2d 272, 205 USPQ (CCPA 1980).

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Okamura (WO 02/065690) in view of Engl et al. (Engl herein after) (US 2003/01442770 A1).

Re Claim 12, Okamura discloses the receiver apparatus as claimed in claim 1 except a quality evaluation circuit. However, Engl teaches a sampling phase control comprising a quality evaluation circuit that evaluates a quality value of the transmitted serial data on the basis of the sampling data ([0064]).

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to utilize the quality evaluation circuit as taught by Engl with the receiver apparatus as taught by Okamura to achieve the same expected results and to further lower the noise in phase for clock generation.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KENNETH LAM whose telephone number is (571)270-1862. The examiner can normally be reached on Mon - Thu 7:30 am - 5:00 pm EST ALT Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Shuwang Liu can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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